Minima Scientist's Corner: International Solid-State Circuits Conference 2018 Reflects Scalable Near-Threshold Voltage Trend

ISSCC covers an incredibly large spectrum of technical areas, of which the most interesting are the forward-looking solutions that may be several years away from being commercialized. For Minima, the most interesting solutions are the ones that are state of the art in very small battery-operated, *intelligent* wireless devices. The wireless sensor ecosystem is marching towards lower supply voltages and supply voltage scalability, the benefits of this are proven time and again, and Minima technology is at the core of this future.

For digital components, Moore's Law has been the number one driver for the last fifty years. For **analog** (including amplifiers, voltage and frequency references, converters, power management), the ride has not been so smooth. All the improvements that drive digital are hindrances in the eyes of analog circuitry: reduction in the range of operating voltages that transistors can handle, as well as their analog performance; simultaneously, transistor parameter variation hits analog (as well as digital). While almost all analog blocks operate at higher voltages than Minima's ultra-low voltages, ISSCC shows that much research has been done in fast power-up and power-down of analog components. Fortunately, near threshold is making gains also in analog. For example, University of Macau, showed a 0.3 to 0.5V crystal oscillator (XO) for Bluetooth Low-Energy (BLE) radios with a steady-state power of less than 32 uW. Pohang University demonstrated a fractional-N ADPLL for DVFS using only a minimum of 653-µW at a supply voltage from 0.3-1.2V with a lock range of 10MHz to 2.7GHz. Impressive gains were made in BLE transceiver power consumption. University of Macau showed an energy-harvesting BLE transmitter operating from just 0.2 V in 28-nm CMOS with an active power of 4 mW and sleep power of just 5.2nW. Next, we need to make near-threshold analog energy scalable to make it compatible with energy-scalable processors.

Continuing with analog components, **power conversion** from battery voltages down to ultra-low voltages and **energy harvesting** techniques always make excellent progress at ISSCC. For energy harvesting, there is a trend toward the use of multiple energy sources at the same time, for example simultaneous photovoltaic, piezoelectric, or thermoelectric transducers. The best harvesters can now harvest sub-microwatt power levels from multiple energy sources at tens of millivolts and these numbers line up perfectly with Minima technology. For example, Oregon State University and Texas Instruments presented a 960pW / 1V output voltage wireless energy harvester powered off 2.4GHz WiFi. This performance would only be improved for lower output voltages such as 0.5V.

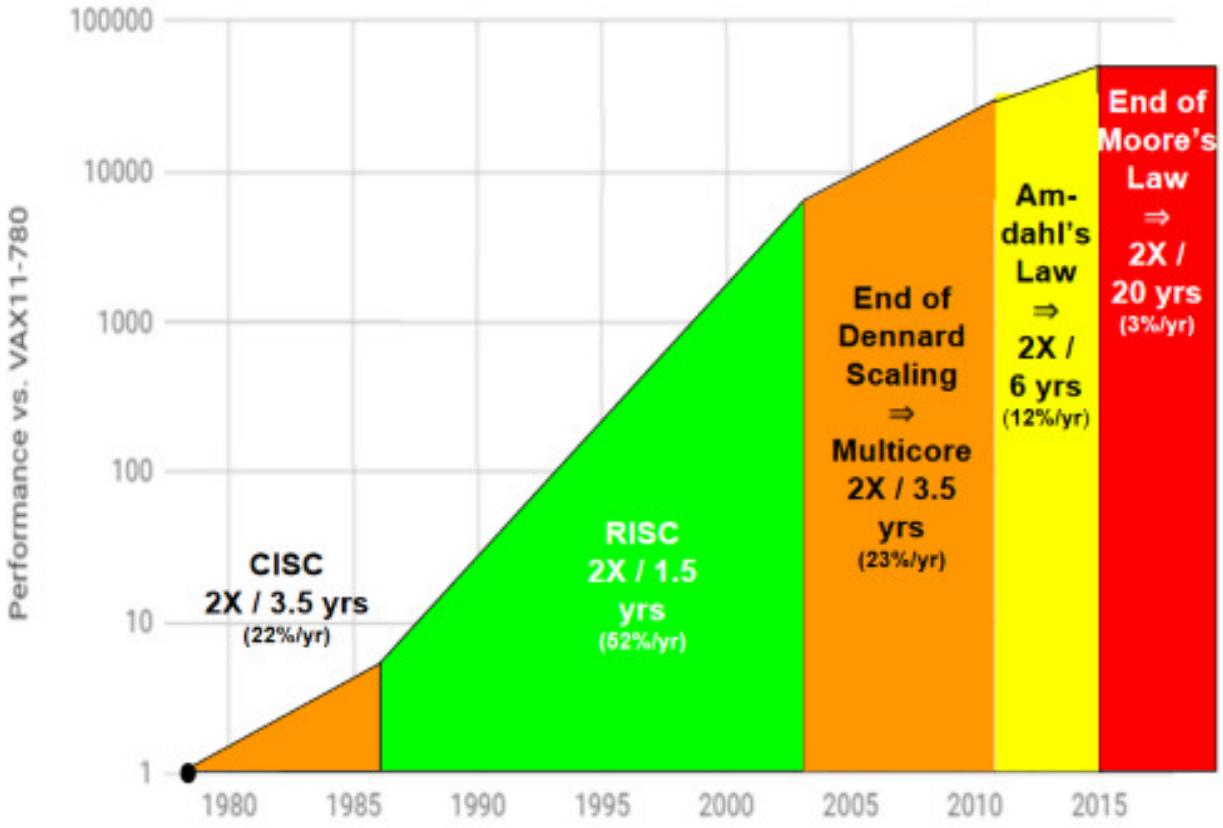
For small wireless end devices, **voltage regulators** have to be integrated on chip to reduce device size (and cost). ISSCC always shows more integration and scaled process nodes with Low-dropout linear regulators (LDOs), switched-capacitor voltage regulators (SCVRs), and this year also inductor-

based buck voltage regulators (LCVRs). Additionally, faster and finer grained conversion is required for Minima's ultra-wide DVFS and ISSCC also delivered new results here. For example, Hanyang University presented a current-mode buck converter with a wide range of output from 0.15V to 1.69V with 1.8V input with peak efficiency of 94.9%. Unfortunately, this converter still requires an off-chip inductor and capacitor. Ohio State University presented a good reference for the upcoming Minima SCVR IP: a fully-integrated switched-C converter with an 100pH on-chip inductor achieving 70.2% efficiency at 0.92 A/mm^2.

In memory circuits, SRAM remains a big part of any IoT end. Samsung showed a 256Mb SRAM array with a minimum voltage below 0.7V. Unfortunately the technology was 7nm FINFET, which is not economical for IoT. One mitigation is that Flash memory can soon be replaced with more efficient alternatives, such as phase-change memory (PRAM), ferroelectric RAM (FeRAM), STT magnetic RAM (STT-MRAM), and Resistive RAM (RRAM). ISSCC showed all of these reaching MB array sizes. An energy-efficiency rethink of end device memory hierarchy is required when the alternative memories become mature.

One big part of future end devices will be machine learning and artificial intelligence. With the emergence of IoT, the amount of data generated will be prohibitive for processing solely in the cloud, both in terms of wireless bandwidth and the amount of energy required to transmit that data. Energy-per-bit ranges from Bluetooth's 50 nJ/bit to Wifi's 5 nJ/bit (yes, Bluetooth is not good in terms of energy, only power) and the emerging NB-IoT standards will not help. Therefore, machine learning will be a big part of end devices and ISSCC delivered new results here as well. Neural-network processor units (NNPUs) execute machine-learning functions faster and with higher energy efficiency than CPUs or GPUs. NNPU trend is toward reduced-precision networks and Kaist from Daejeon, Korea, presented a deep neural network accelerator with 1b-to-16b variable bit-weight precision. Such variable bit weights are perfect for implementing with Minima's Dynamic Margining solution.

Finally, Dave Patterson gave an awesome plenary talk about processor history and Google's Tensorflow Processor Unit (I didn't know that Dave was behind Tensorflow, but it didn't surprise me at all). I appreciated how he described the various business decisions along with the technical decisions behind the various architectures (CISC, RISC, etc.) and did not pull punches (Itanium VLIW). ISSCC is inspiring in how it delves into semiconductor history and simultaneously presents the future.



Dave Patterson showed that Intel CPU performance has plateaued at just three percent/year. Source: Computer Architecture: A Quantitative Approach, 2018.